ABSTRACT

In Very Large Scale Integration (VLSI) design, the devices require compact area, low power and high speed circuits. Digital Signal Processing (DSP) building blocks which are widely used in computing and communication fields need such efficient circuit design. Though many efforts have been made in improvement of the system design to satisfy the requirements, it is still to be improved further. In this thesis, architectures have been proposed to improve the performance of the Discrete Cosine Transform (DCT) in terms of power, area and speed. As the DCT is a commonly used block set in signal processing applications, the improvement in the performance of the DCT will be of great significance.

The first method is based on Vedic algorithm for multiplication and carry select adder (CSA) for addition. It is primarily developed to enhance the speed of DCT. This technique would reduce the delay of the system. Conventional DCT and algorithm-architecture transformation of DCT with array multiplier and ripple carry adder (RCA) is redesigned with Vedic multiplier and carry select adder. The 8-point DCT architectures are designed and implemented by using Xilinx Spartan 3E Field Programmable Gate Array (FPGA).

The synthesis results show that the combinational delay and power for Vedic multiplier is reduced by 36% and 12% respectively than the conventional array multiplier. The combinational delay and power of CSA is reduced by 24% and 2% respectively than RCA with almost same power.

The performance of the proposed Vedic DCT reduces the delay around 8% with an increase of 12% in the additional area than conventional DCT. Even though the performance of the proposed Vedic algorithm-

architecture transformation DCT reduces the delay around 47%, it occupies 6% of additional area than conventional algorithm-architecture transformation DCT. Power is reduced slightly in addition to delay which makes the architecture efficient.

The second method suggested in this study is reversible logic. Reversible computing has emerged as a promising technology in reducing power dissipation. An n input and n output functions are said to be reversible, if there are same number of inputs and outputs. Also the input vector can always be determined from its output vector. This technique is applied to DCT and implemented in Xilinx Spartan 3E FPGA.

The proposed DCT using reversible logic reduces the power consumption by 10% whereas it increases the area and delay by 24% and 1.5% respectively when compared to the conventional DCT.

The third approach is to design the VLSI architecture for Discrete Cosine Transform using Gate Diffusion Input (GDI) technique. This technique is suitable for low-power, high speed circuits using reduced number of transistors. An existing 10 transistor full adder circuit is used for addition. The conventional DCT is realized with GDI adders and multipliers.

A modified full adder circuit using GDI technology is developed with only 8 transistors (8T) which replaces the 10 transistors (10T) full adder in DCT architecture. GDI DCT further improves the structural simplicity by its recursive structures though it optimizes energy efficiency.

Simulations have been performed on Tanner SPICE for 90nm Complementary Metal Oxide Semiconductor (CMOS) process technology at 100 MHZ. Area and powers are reduced by 21.26% and 21.23% respectively

and delay is reduced by 19.5% in GDIDCT than the conventional DCT. Area, power and delay of 8T GDI adder DCT are reduced by 10.3%, 28.6% and 11.1% respectively than existing 10T GDI adder DCT.

The fourth method is approximate DCT using GDI technique. Mostly the problems encountered in using DSP circuits are computational complexity, increased power consumption and low speed of operation. These issues can be overcome by using approximate DCT architecture. The perception of human visualization permits in designing approximate rather than exact DCT. The 8-point 1D approximate DCT architecture requiring 14 additions and 12 additions for realization is designed by using 8T GDI Full adder. For DCT using 14 additions, area, power and delay are reduced by 95%, 99 % and 95% respectively and for DCT using 12 additions area, power and delay are further reduced by 23%, 16.6% and 12% respectively than GDIDCT using 14 additions.

The approximate DCT architecture is extended for 16-point. Larger size 16/32-point DCT is in current and subsequent generation video standard. To fulfill this requirement, this work proposes a fast computation intensive architecture for large size DCT. The 16-point extension of 8-point approximate DCT architecture using 12 additions reduce the area, power and delay by 20.8%, 16.9% and 10.3% respectively than 16-point extension of 8-point approximate DCT architecture using 14 additions .

An 8 or 16-point Approximate 1D DCT architecture is useful for transforming one dimensional signal like speech. But the two dimensional signals like image and video need 2D DCT for its processing. So an Approximate MGDI 2D DCT is designed by using 8T GDI adder. The simulation result shows that 13.9% of area, 15.08 % of power and 7% of delay are reduced in the 8-point approximate 2D DCT. The area, power and

delay of 16-point approximate 2D DCT using8T GDI adder are reduced by 10.63 %, 15.48% and 8% respectively. The proposed architecture enhances results in terms of hardware complexity, regularity and modularity with a little compromise in accuracy.